FOUNDER

eMMC 32GB
MKEV032GCB-SS510
Specification

V1.0

May 10, 2019

Contents

List of Figures

List of Table

1. Foreword

This document has been produced by MKEV032GCB-SS510 , should the company modifies the contents of this specification, it will be re-released with an identifying change of release date and an increase in revision number as follows:

Revision mn.xy, where:

- mn the first two digit are incremented for major changes of substance, e.g., functional changes.
- xy the second two digits are incremented when minor changes have been incorporated into the specification, i.e., enhancements, corrections, updates, etc.

Top page

2. Revision History

Revision	Date	Modified By	Description
1.0	2019/05/10	Ian Lin	Initial release

Top page

3. Statement of Scope

This Datasheet document is described the eMMC MKEV032GCB-SS510 of methods and abstractions of reliability. The contents include the concept and measurement methodologies.

Top page

4. General Description

MKEV032GCB-SS510 e•MMC is an embedded storage solution designed in a BGA package form. The operation of e•MMC is compatible with e•MMC 5.1 which is an industry standard.

The e•MMC consists of NAND flash and a controller. 3.3V supply voltage is required for the NAND area (VCC)， whereas 1.8V or 3.3V dual supply voltage is supported for the interface.

There are several advantages of e•MMC. It is easy to be used on the standard interface, which allows the easy and widely used integration with general CPU. Any revision or amendment of NAND is invisible to the host as the embedded e•MMC controller insulates NAND technology from the host. It means that the host can support the newest processing flash without updating its hardware or software.

MKEV032GCB-SS510 e•MMC has high performance at a competitive-cost, high quality and low power consumption. e•MMC provides capacities from 4GB to 64GB.

4.1. Product list

Table 4- 1 eMMC product list

Capacities	Part Number	Flash Type	User Density	Package Size (mm)	Package Type
32GB	MKEV032GCB-SS510	256Gb TLCx1	91.5 %	11.5x13x1.0	153FBGA

Top page

4.2. Feature

- Compatible to JEDEC Embedded Multi-Media Card (e•MMC) Electrical Standard (5.1)
- Data bus width: 1bit, 4bit and 8bit.
- Power-down safeguard
- Hardware ECC engine

- Unique firmware backup mechanism
- Global wear leveling to expend NAND flash endurance
- IDA（Initial Data Accelerating）
- Backward Compatible with JEDEC standard
- Supports HS400 mode

Top page

5. Functional Description

MKEV032GCB-SS510 e•MMC with powerful L2P NAND Flash management algorithm provides unique functions:

- Host independence from details of operating NAND flash.
- Internal ECC to correct defect in NAND flash.
- Power-down safeguard.

  To prevent from false operating, a mechanism named power-down safeguard is added in the e•MMC. In the case of sudden power-losing, the e•MMC would work properly when it gets power again.
- Global wear leveling.

  To achieve the best stability and device endurance, this e•MMC equips the Global Wear Leveling algorithm. It ensures that not only normal area, but also the frequently accessed area, such as FAT, would be programmed and erased evenly.
- IDA（Initial Data Accelerating）

  IDA may accelerate the Initial data written to the e•MMC, saving the time up to 50% off in the downloading process.

Top page

6. Product Specifications

6.1. Performance (Typical Value)

Table 6- 1 Performance (Typical Value)

Part Number	Capacity	Interleave Operation	Mode	SLC Sequential Write (MB/s)	Sustained Sequential (MB/s)	
					Read	Write
MKEV032GCB-SS510	32GB	I0	HS400	120	260	18

Test Condition: Bus width x8, 200MHz DDR, 512KB data transfer, w/o file system overhead, measured on internal board.

Top page

6.2. Electrical Characteristics

General

Table 6- 2 Electrical Characteristics- General

Parameter	Symbol	Test Conditions	Min.	Max.	Unit
Peak voltage on all lines	-	-	-0.5	V_{CCQ}+0.5	V
All Inputs					
Input Leakage Current (before initialization sequence1 and/or the internal pull up resistors connected)	-	-	-100	100	μA
Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)	-	-	-2	2	μA
All Outputs					
Output Leakage Current (before initialization sequence)	-	-	-100	100	μA
Output Leakage Current (after initialization sequence)	-	-	-2	2	μA

Note* :

Initialization sequence is defined in Power-Up chapter of JEDEC/MMCA Standard.

Power Supply Voltage

Table 6- 3 Power Supply Voltage

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply voltage 1 (NAND)	V_{CC}	2.7	3.6	V	
Supply voltage 2 (I/O)	V_{CCQ}	2.7	3.6	V	
		1.7	1.95		

Supply Current

Table 6- 4 Supply Current

Parameter		Symbol	Interleave	Mode	VccQ	ICCQ (Max)	Unit
Operation (RMS)	Read	IROP	Non Interleave	SDR	1.8V	100	mA
					3.3V	100	
				DDR	1.8V	115	mA
					3.3V	120	
				HS200	1.8V	150	mA
				HS400	1.8V	250	mA
	Write	IWOP	Non Interleave	SDR	1.8V	60	mA
					3.3V	60	
				DDR	1.8V	75	mA
					3.3V	80	
				HS200	1.8V	120	mA
				HS400	1.8V	120	mA

Internal resistance and Device capacitance

Table 6- 5 Internal resistance and Device capacitance

Parameter	Symbol	Test	Min	Max	Unit
Single device capacitance	C_{DEVICE}			6	pF
Internal pull up resistance DAT1 – DAT7	R_{INT}		10	150	KΩ

Bus Signal Levels

Figure 6- 1 Bus Signal Levels

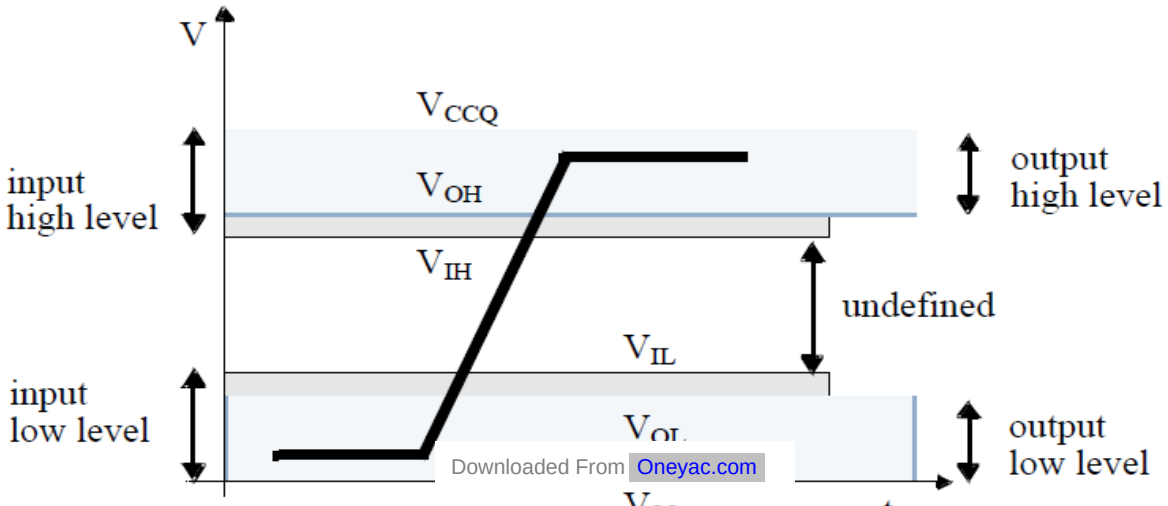


Table 6- 6 Bus Signal Levels

Parameter	Symbol	Test Conditions	Min.	Max.	Unit
Open-Drain Mode Bus Signal Level					
Output HIGH voltage	V_{OH}	I_{OH} = -100uA	VccQ - 0.2		V
Output LOW voltage	V_{OL}	I_{OL} = 2mA		0.3	V
Push-Pull Mode Bus Signal Level (High-Voltage)					
Output HIGH voltage	V_{OH}	IOH = -100uA @ VDD min	0.75*V_{CCQ}		V
Output LOW voltage	V_{OL}	IOL = 100uA @ VDD min		0.125* V_{CCQ}	V
Input HIGH voltage	V_{IH}		0.625* V_{CCQ}	V_{CCQ} + 0.3	V
Input LOW voltage	V_{IL}		V_{SS} - 0.3	0.25* V_{CCQ}	V
Push-Pull Mode Bus Signal Level (Dual-Voltage)					
Output HIGH voltage	V_{OH}	I_{OH} = -2mA @ VDD min	V_{CCQ} - 0.45		V
Output LOW voltage	V_{OL}	I_{OL} = 2mA @ VDD min		0.45	V
Input HIGH voltage	V_{IH}		0.65* V_{CCQ}	V_{CCQ} + 0.3	V
Input LOW voltage	V_{IL}		V_{SS} - 0.3	0.35* V_{CCQ}	V

Top page

6.3. Product Architecture

Figure 6- 2 Product Architecture

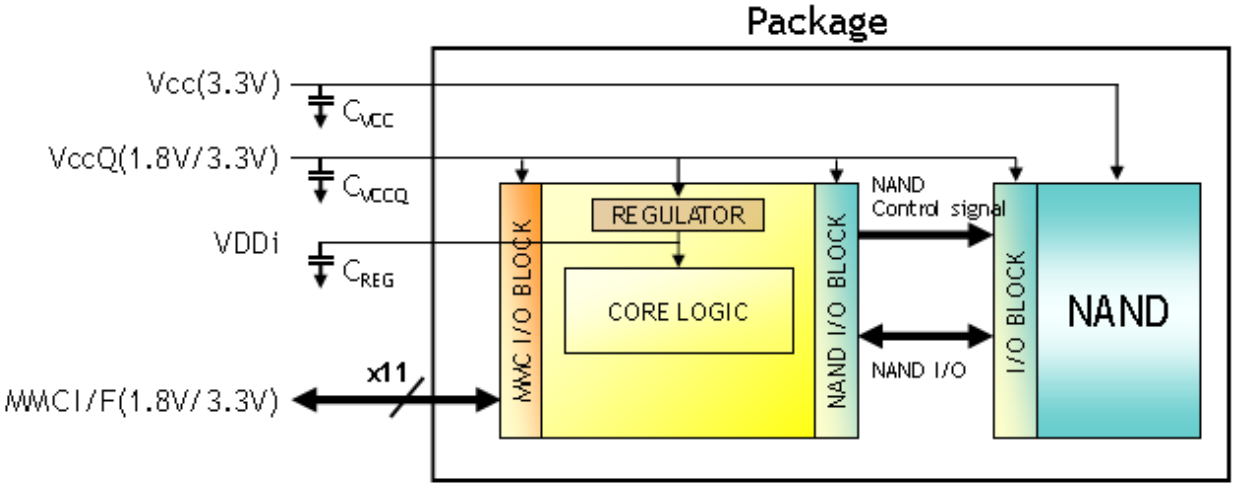


Table 6- 7 Product Architecture

Parameter	Symbol	Unit	Min.	Typ.	Max.
VDDi capacitor value	C_{REG}	uF	0.1	1	2.2
V_{CC} capacitor value	C_{VCC}	uF	-	2.2+0.1	-
$V_{CC}Q$ capacitor value	C_{VCCQ}	uF	-	2.2+0.1	-

Note* :
e•MMC recommends that the minimum value should be usually applied as the value of CREG; CREG shall be compliant with X5R/X7R of EIA standard or B of JIS standard.

Top page

6.4. Operational Environment

Table 6- 8 Operational Environment

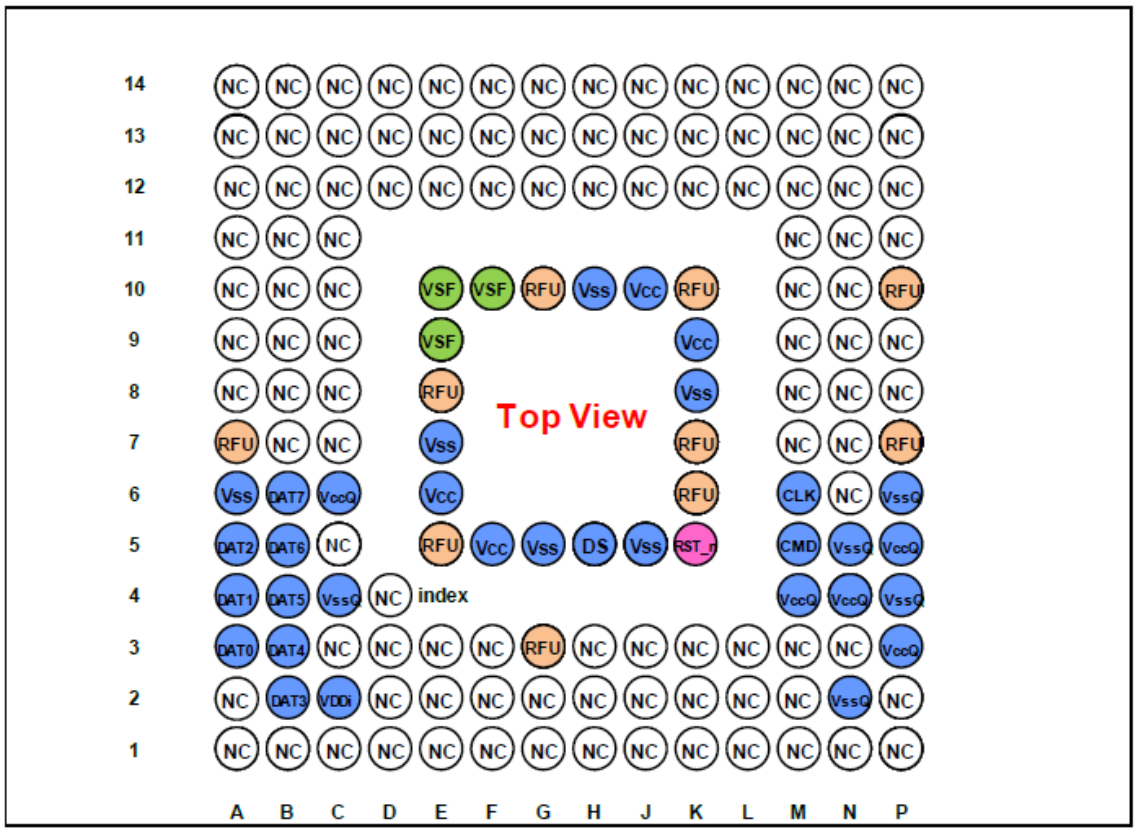
Mode	Temperature
Operating	-25℃ to 85℃
Storage without operation	-40℃ to 85℃

Top page

7. Package Configurations

7.1. eMMC 153 Ball Array view

Figure 7- 1 eMMC 153 ball Array view (Top view)



Top page

7.2. eMMC Pin Description

Table 7- 1 eMMC Pin Description

Pin Number	Name	Pin Number	Name	Pin Number	Name	Pin Number	Name
A3	DAT0	C2	VDDi	J5	VSS	N4	VCCQ
A4	DAT1	C4	VSSQ	J10	VCC	N5	VSSQ
A5	DAT2	C6	VCCQ	K5	RSTN	P3	VCCQ
A6	VSS	E6	VCC	K8	VSS	P4	VSSQ
B2	DAT3	E7	VSS	K9	VCC	P5	VCCQ
B3	DAT4	F5	VCC	M4	VCCQ	P6	VSSQ
B4	DAT5	G5	VSS	M5	CMD		
B5	DAT6	H5	DS	M6	CLK		
B6	DAT7	H10	VSS	N2	VSSQ		

Note* :
NC: No Connect, can be connected to ground or left floating.
RFU: Reserved for Future Use, should be left floating for future use.
VSF: Vendor Specific Function, shall be left floating.

Top page

7.3. eMMC Pin Assignment

Table 7- 2 eMMC Pin Assignment

Signal	Description
CLOCK (CLK)	Each cycle of the clock directs a transfer on the command line and on the data lines. The frequency can vary between the minimum and the maximum clock frequency.
COMMAND (CMD)	This signal is a bidirectional command channel used for device initialization and command transfer. The CMD Signal has 2 operation modes: open drain, for initialization, and push-pull, for command transfer. Commands are sent from the host to the device, and responses are sent from the device to the host.

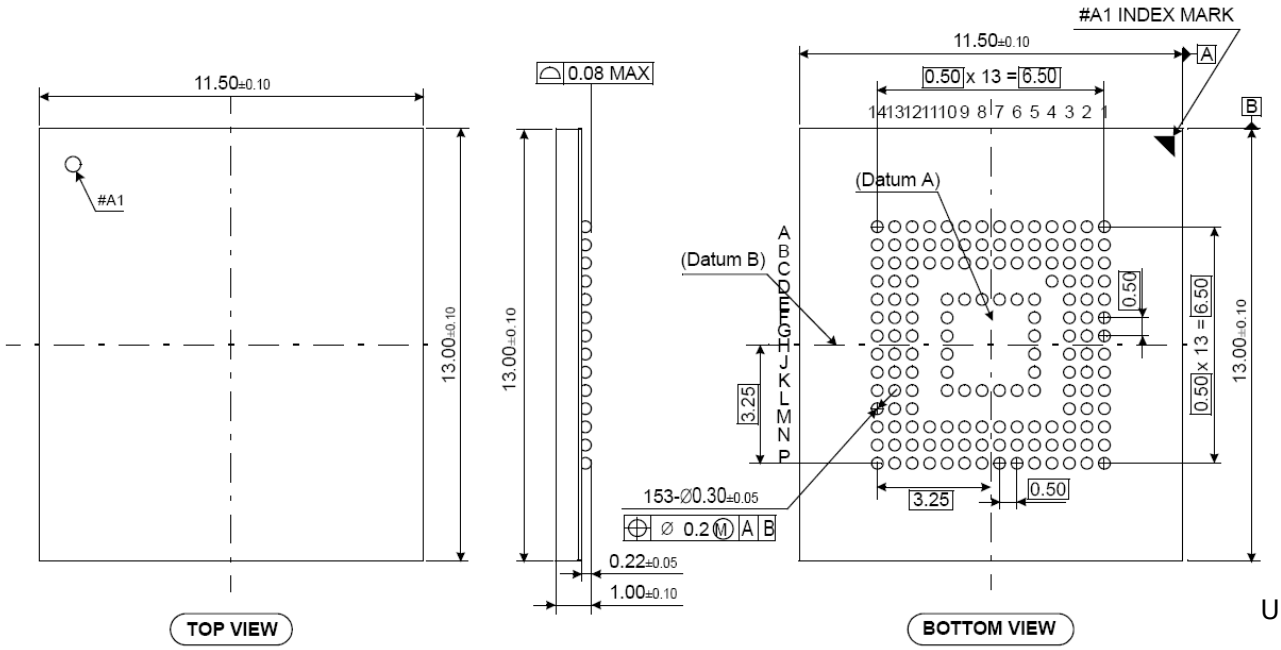
DATA (DAT0-DAT7)	These are bidirectional data signal. The DAT signals operate in push-pull mode. By default, after power-up or RESET, only DAT0 is used for data transfer. The controller can configure a wider data bus for data transfer withers using DAT [3:0] (4bit mode) or DAT [7:0] (8bit mode). Includes internal pull-up resistors for data lines DAT [7:1]. Immediately after entering the 4-bit mode, the device disconnects the internal pull-up resistors on the DAT1 and DAT2 lines.(The DAT3 line internal pull-up is left connected.)Upon entering the 8bit mode, the device disconnects the internal pull-up on the DAT1, DAT2, and DAT[7:4] lines.
RESET (RSTN)	Hardware Reset Input
DS	Data Strobe: Return Clock signal used in HS400 mode
VCCQ	VCCQ is the power supply line for host interface, have two power mode: High power mode:2.7V~3.6V; Lower power mode:1.7V~1.95V
VCC	VCC is the power supply line for internal flash memory, its power voltage range is:2.7V~3.6V
VDDi	VDDi is internal power node, not the power supply. Connect 0.1uF or 1uF capacitor VDDi to ground
VSS,VSSQ	Ground lines.

Note* : All other pins are not connected [NC] and can be connected to GND or left floating.

Top page

7.4. 153 Ball Pin Configuration

Figure 7- 2 eMMC 153 ball Pin Configuration



Unit: mm

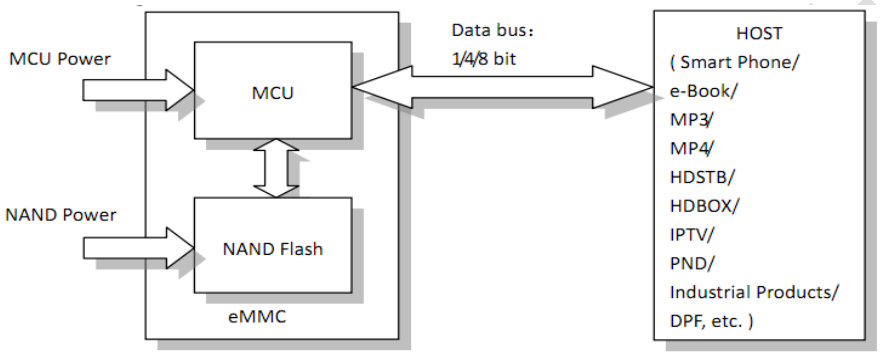
11.5mm×13mm×1.0mm Package Dimension

8. Usage Overview

8.1. General Description

The e•MMC can be operated in 1, 4, or 8-bit mode. NAND flash memory is managed by a controller inside, which manages ECC, wear leveling and bad block management. e•MMC provides easy integration with the host process that all flash management hassles are invisible to the host.

Figure 8- 1 Device Power Diagram



Top page

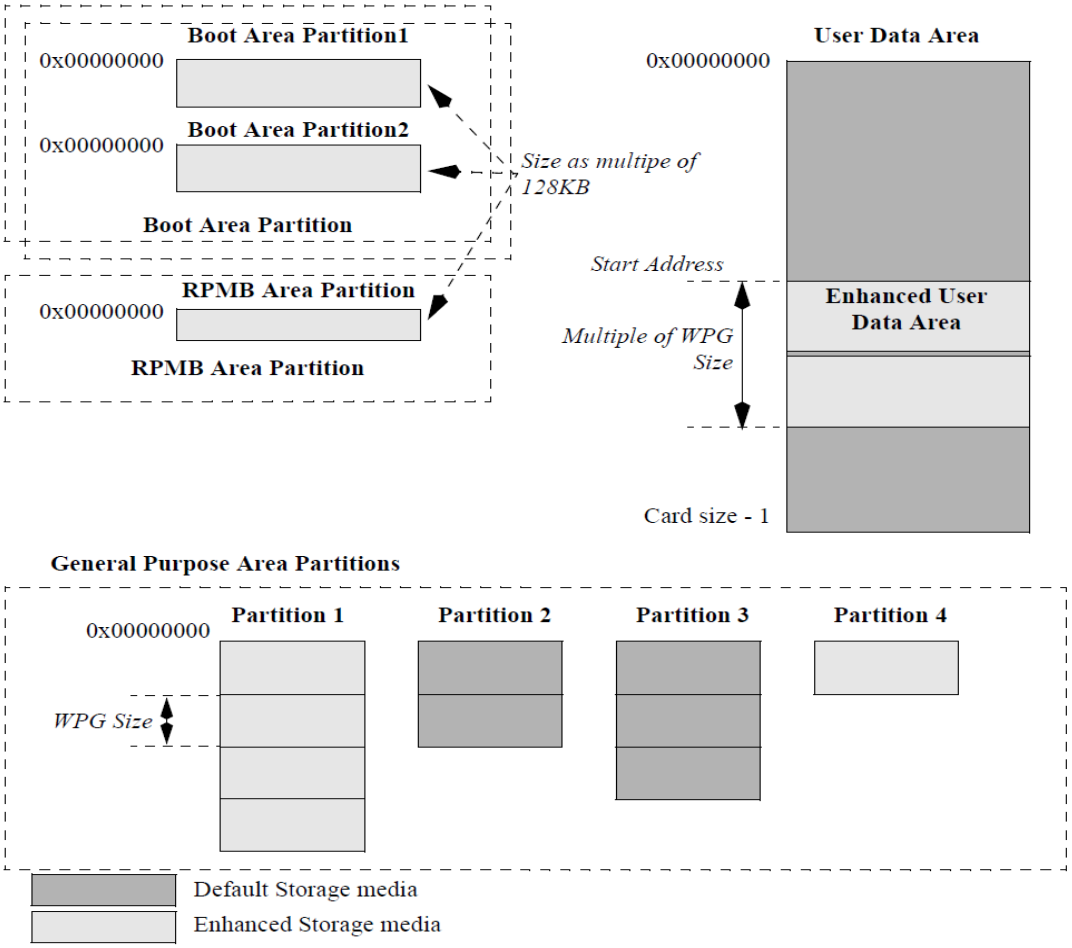
8.2. Partition Management

The embedded device offers also the possibility of configuring by the host additional split local memory partitions with independent addressable space starting from logical address 0x00000000 for different usage models. Default size of each Boot Area Partition is 128 KB and can be changed by Vendor Command as multiple of 128KB. Boot area partition size is calculated as (128KB * BOOT_SIZE_MULTI) The size of Boot Area Partition 1 and 2 cannot be set independently and is set as same value Boot area partition which is enhanced partition. Therefore memory block area scan is classified as follows:

- Factory configuration supplies boot partitions.
- The host is free to configure one segment in the User Data Area to be implemented as enhanced storage media, and to specify its starting location and size in terms of Write Protect Groups. The attributes of this Enhanced User Data Area can be programmed only once during the device life-cycle (one-time programmable).

- Up to four General Purpose Area Partitions can be configured to store user data or sensitive data, or for other host usage models. The size of these partitions is a multiple of the write protect group. Size and attributes can be programmed once in device life-cycle (one-time programmable). Each of the General Purpose Area Partitions can be implemented with enhanced technological features.

Figure 8- 2 Partitions and user data area configuation



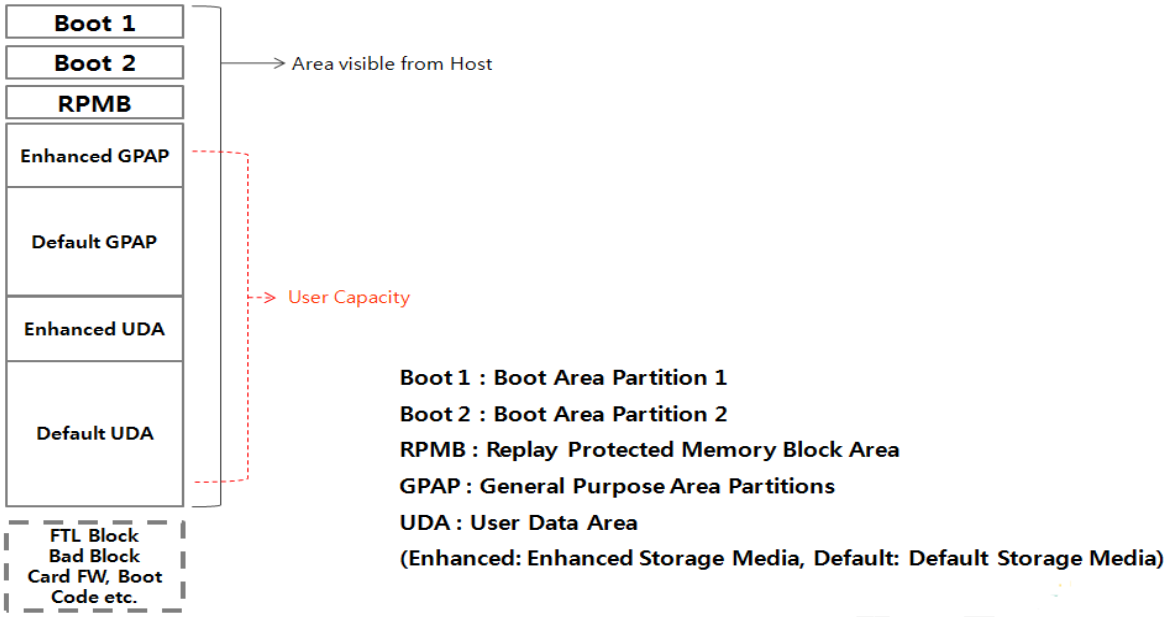


Table 8- 1 Partition Configuration Table

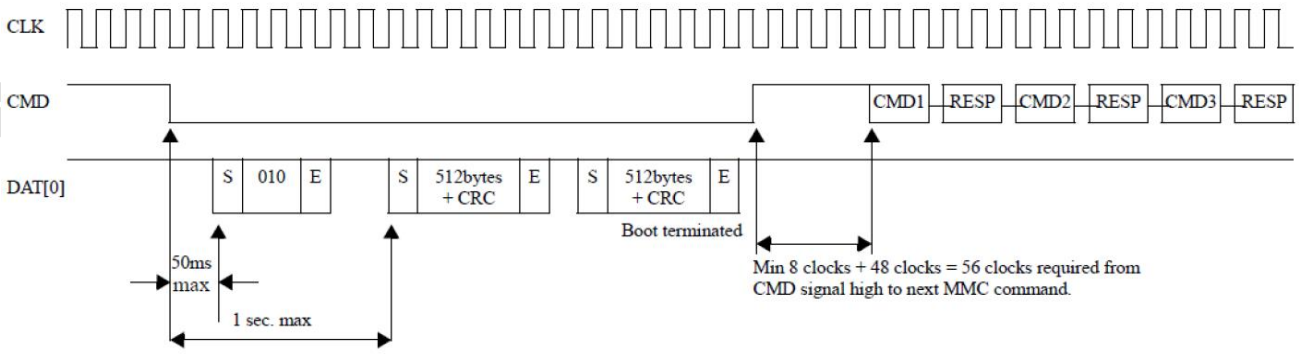
Boot1 Size	Boot2 Size	RPMB Size
4MB	4MB	4MB

Top page

8.3. Boot operation mode

In boot operation mode, the master can read boot data from the slave (device) by keeping CMD line low or sending CMD0 with argument + 0xFFFFFFFA, before issuing CMD1. The data can be read from either boot area or user area depending on register setting.

Figure 8- 3 Boot operation mode



State diagram (boot mode)
Boot operation complete Clock = 400 kHz
(Compatible with the description which ≤400kHz)

Figure 8- 4 State diagram (alternative boot mode)

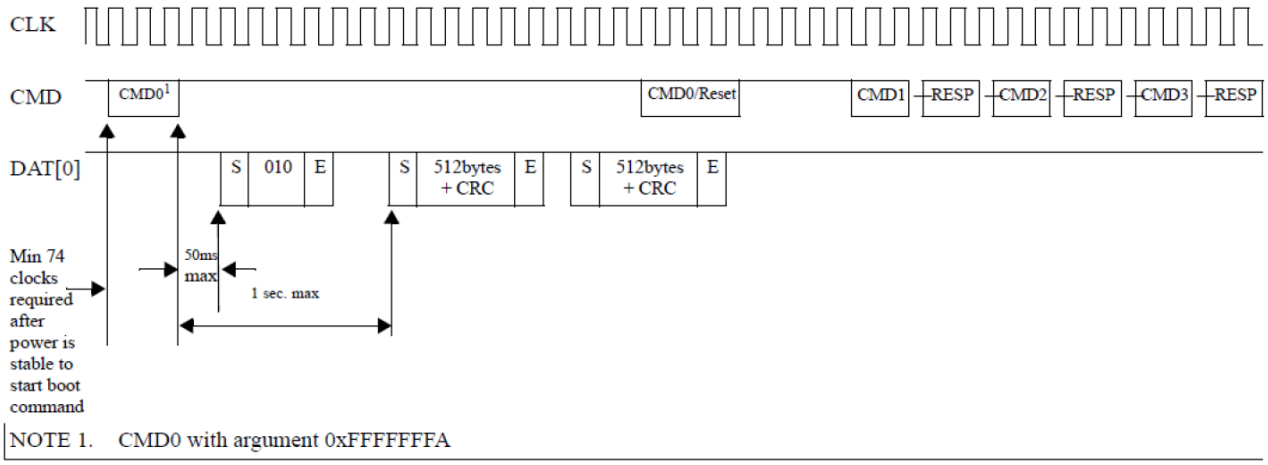
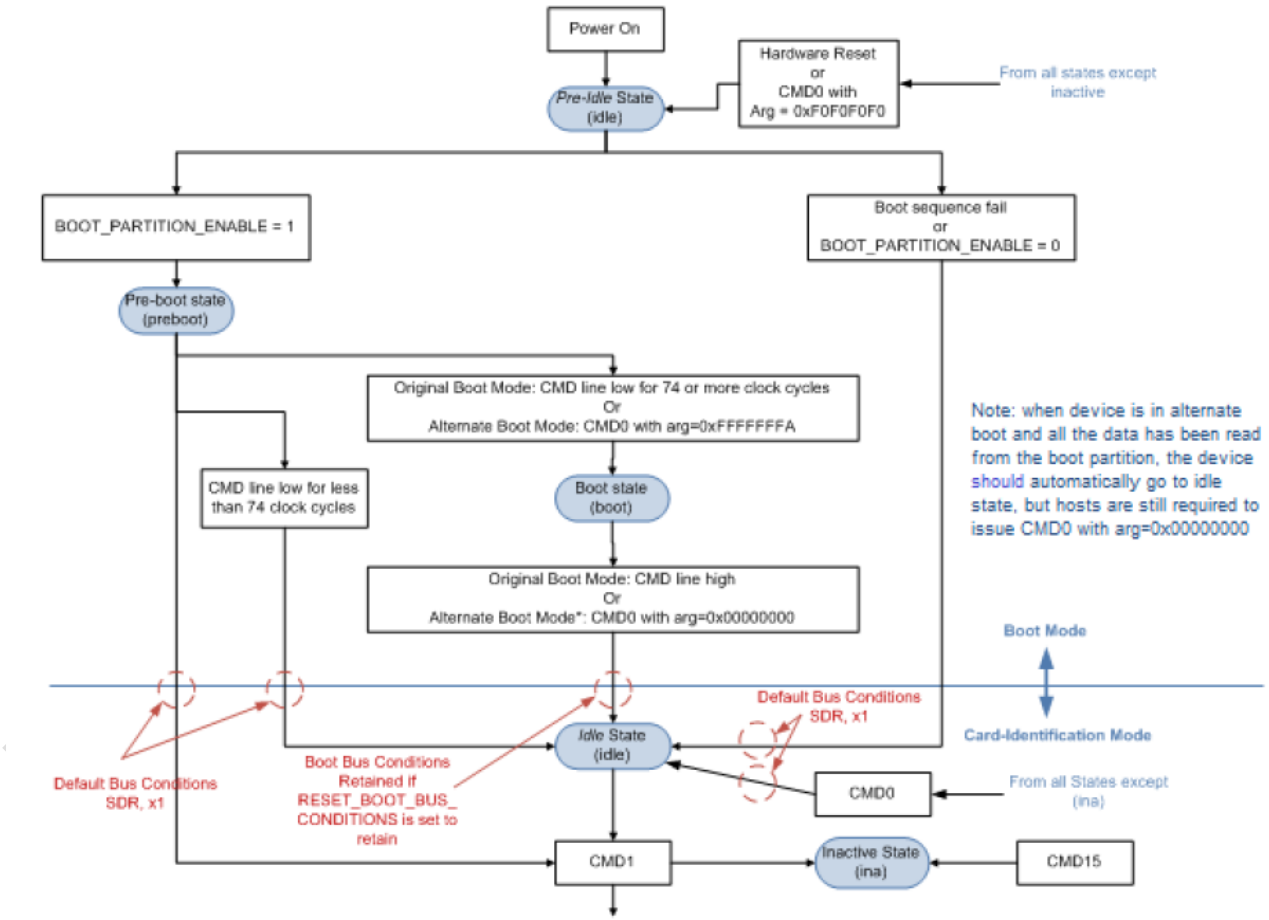


Figure 8- 5 State diagram (boot mode)

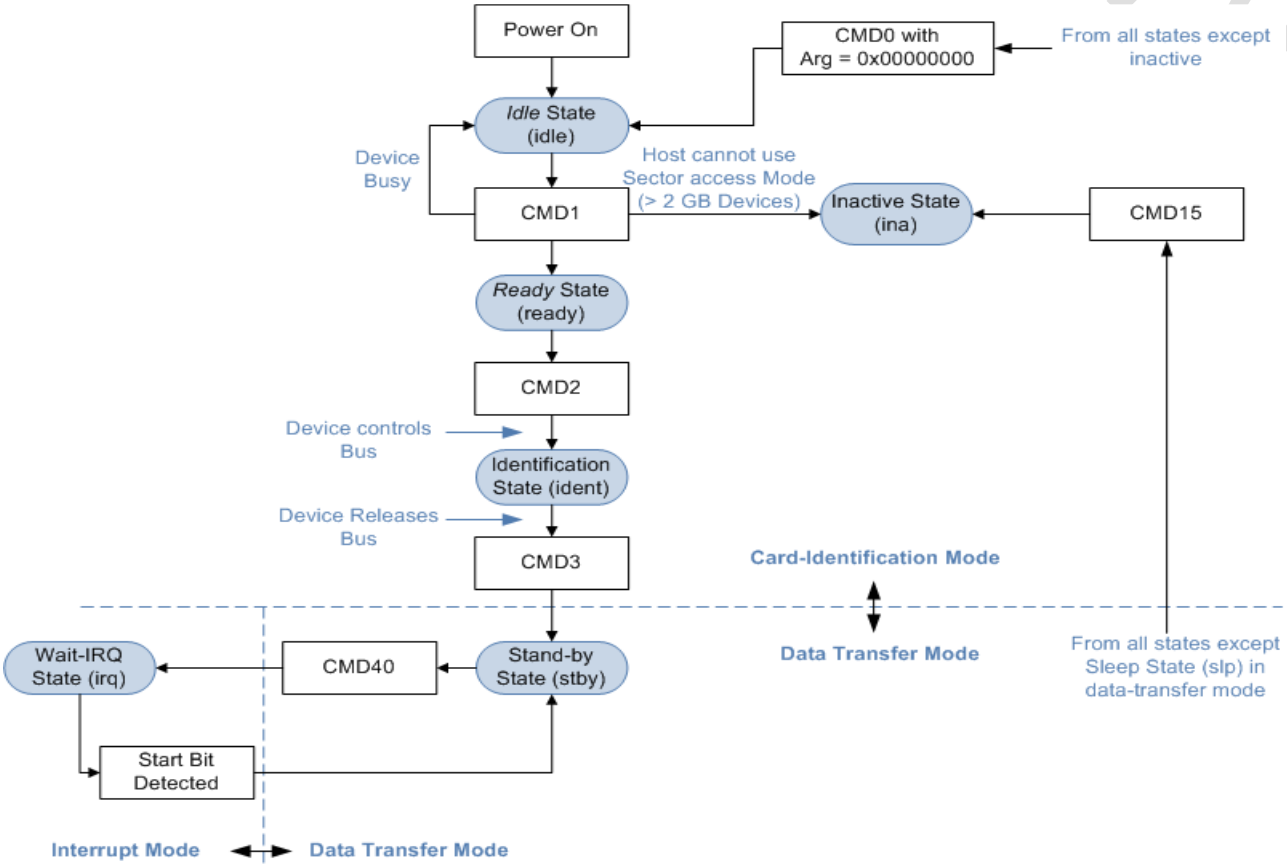


Top page

8.4. Device identification mode

While in device identification mode the host resets the device, validates operation voltage range and access mode, identifies the device and assigns a Relative device Address (RCA) to the device on the bus. All data communication in the Device Identification Mode uses the command line (CMD) only.

Figure 8- 6 State diagram (card identification mode)

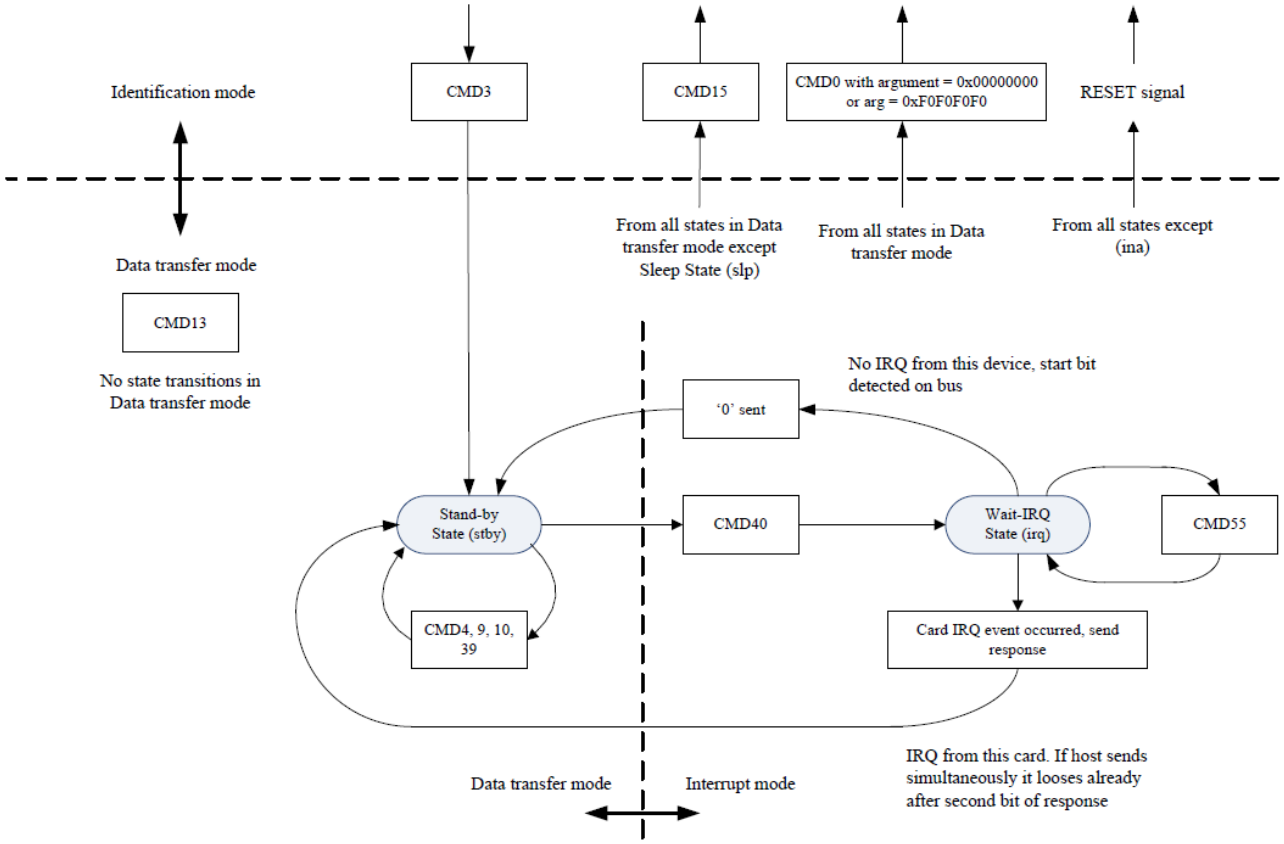


Top page

8.5. Interrupt mode

The interrupt mode on the system enables the master (host) to grant the transmission allowance to the slaves (card) simultaneously. This mode reduces the polling load for the host and hence, the power consumption of the system, while maintaining adequate responsiveness of the host to a card request for service. Supporting interrupt mode is an option, both for the host and the card.

Figure 8- 7 State transition diagram, interrupt mode



Top page

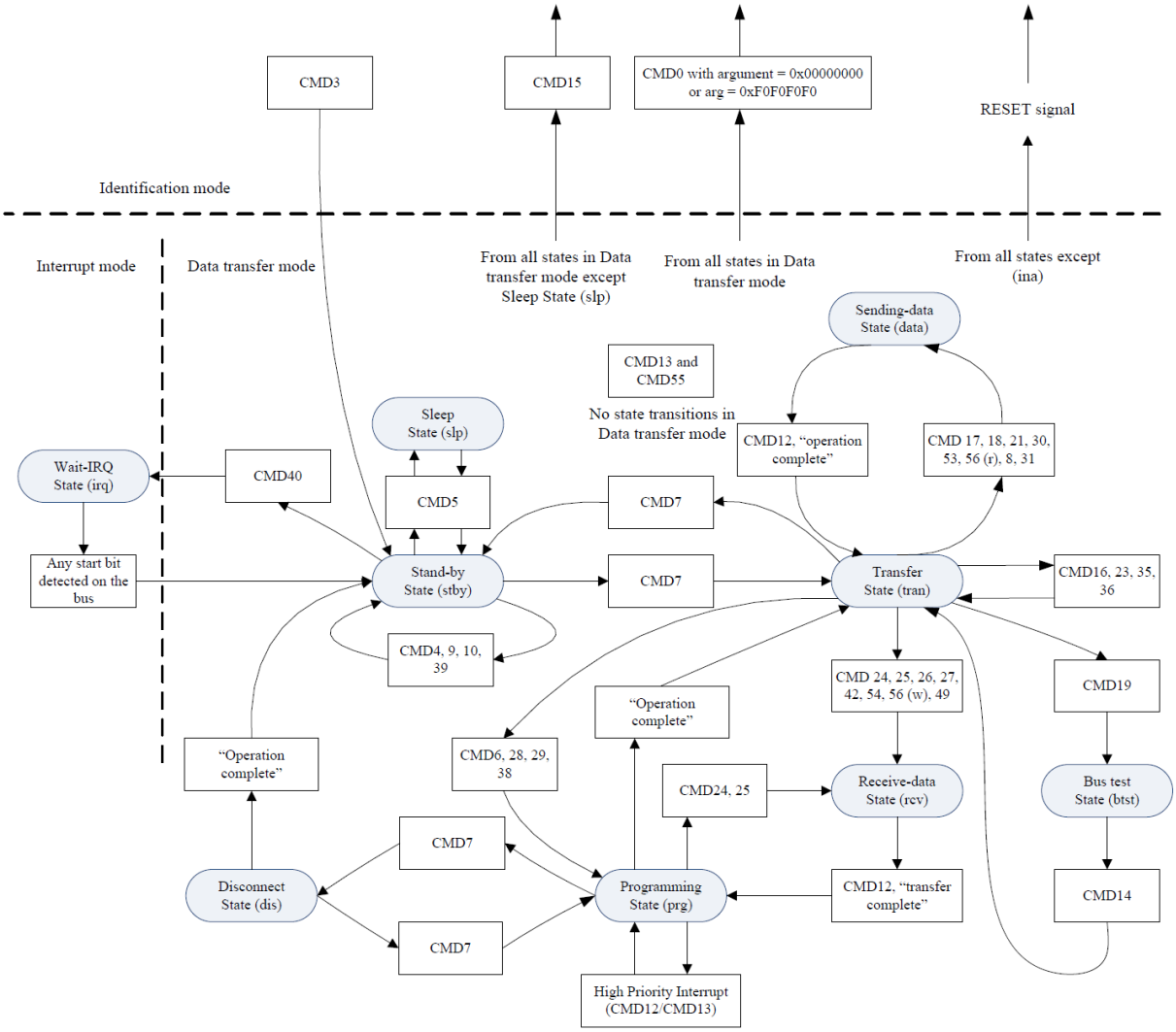
8.6. Data transfer mode

All data communication in the Data Transfer Mode is point-to point between the host and the selected card (using addressed commands). All addressed commands get acknowledged by a response on the CMD line.

While the card is in Stand-by State, CMD7 is used to select the card and put it into the Transfer State by including card's relative address in the argument. If the card was previously selected and was in Transfer State its connection with the host is released and it will move back to the Stand-by State when deselected by CMD7 with any address in the argument that is not equal to card's own relative address. When CMD7 is issued with the reserved relative card address "0x0000", the card is put back to Stand-by State. Reception of CMD7 with card's own relative address while the card is in Transfer State is ignored by the card and may be treated as an Illegal Command. After the card is assigned an RCA it will not respond to identification commands — CMD1, CMD2, or CMD3.

While the card is in Disconnect State, CMD7 is used to select the card and put it into the Programming State by including card's relative address in the argument. If the card was previously selected and was in Programming State its connection with the host is released and it will move back to the Disconnect State when deselected by CMD7 with any address in the argument that is not equal to card's own relative address. Reception of CMD7 with card's own relative address while the card is in Programming State is ignored by the card and may be treated as an Illegal Command.

Figure 8- 8 State diagram (data transfer mode)



Top page

8.7. High Priority Interrupt

The high priority interrupt (HPI) mechanism enables servicing high priority requests, by allowing the device to interrupt a lower priority operation before it is actually completed, within OUT_OF_INTERRUPT _TIME timeout. Host may need to repeat the interrupted operation or part of it to complete the original request. The HPI command may have one of two implementations in the device:

- CMD12 – based on STOP_TRANSMISSION command when the HPI bit in its argument is set.

- CMD13 – based on SEND_STATUS command when the HPI bit in its argument is set.

Host shall check the read-only HPI_IMPLEMENTATION bit in HPI_FEATURES (EXT_CSD byte [503]) and use the appropriate command index accordingly.

CMD Index	Name	Is interruptible?
CMD24	WRITE_BLOCK	Yes
CMD25	WRITE_MULTIPLE_BLOCK	Yes
CMD38	ERASE	Yes
CMD6	SWITCH, byte BKOPS_START, any value	Yes
CMD6	SWITCH, byte SANITIZE_START, any value	Yes
CMD6	SWITCH, byte POWER_OFF_NOTIFICATION, value POWER_OFF_LONG or SLEEP_NOTIFICATION	Yes
CMD6	SWITCH, byte POWER_OFF_NOTIFICATION, other values	No
CMD6	CACHE_CTRL when used for turning the cache OFF	Yes
CMD6	FLUSH_CACHE	Yes
CMD6	SWITCH, other bytes, any value	No
All others		No

Top page

8.8. High-speed mode selection

After the host verifies that the Device complies with version 4.0, or higher, of this standard, it has to enable the high speed mode timing in the Device, before changing the clock frequency to a frequency between 26MHz and 52MHz. For the host to change to a higher clock frequency, it has to enable the high speed interface timing. The host uses the SWITCH command to write 0x01 to the HS_TIMING byte, in the Modes segment of the EXT_CSD register. If the host tries to write an

invalid value, the HS_TIMING byte is not changed, the high speed interface timing is not enabled, and the SWITCH_ERROR bit is set.

Top page

8.9. HS200 timing mode selection

HS200 is valid only at VCCQ= 1.8 V.
The bus width is set to SDR 4bit or SDR 8bit in HS200 mode.
After the host initializes the device, it must verify that the device supports the HS200 mode by reading the DEVICE_TYPE field in the Extended CSD register. Then it may enable the HS200 timing mode in the device, before changing the clock frequency to a frequency higher than 52MHz.
After power-on or software reset(CMD0), the interface timing of the device is set as the default "Backward Compatible Timing ". Device shall select HS200 Timing mode if required and perform the Tuning process if needed.

Top page

8.10. HS400 timing mode selection

The valid IO Voltage for HS400 is 1.8V for VCCQ.

The bus width is set to only DDR 8bit in HS400 mode.

HS400 supports the same commands as DDR52.

After the host initializes the device, host check whether the device supports the HS400 mode by reading the DEVICE_TYPE field in the Extended CSD register. Then it enables the HS400 mode in the device before changing the clock frequency to a frequency higher than 52 MHz. After power-on or software reset (CMD0), the interface timing of the device is set as the default "Backward Compatible Timing".

Top page

8.11. Bus width selection

After the host has verified the functional pins on the bus it should change the bus width configuration accordingly, using the SWITCH command. The bus width configuration is changed by writing to the BUS_WIDTH byte in the Modes Segment of the EXT_CSD register (using the SWITCH command to do so). After power-on, or software reset, the contents of the BUS_WIDTH byte is 0x00.

If the host tries to write an invalid value, the BUS_WIDTH byte is not changed and the SWITCH_ERROR bit is set. This register is written only.

Top page

9. Timing

9.1. Time Out

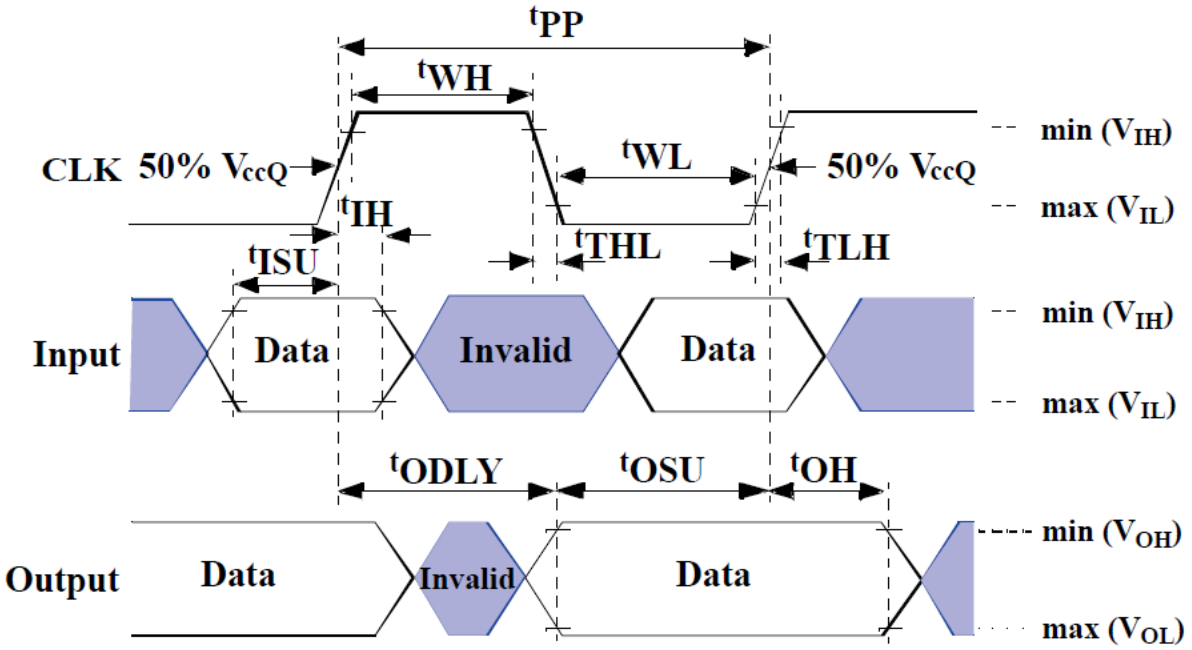
Table 9- 1 Time Out Table

Timing parameter	Value
Read timeout	100 ms
Write timeout	350 ms
Erase timeout	600 ms
Force erase timeout	3 min
Trim timeout	300 ms
Partition switching time out (after init)	30 ms

Top page

9.2. Bus Timing

Figure 9- 1 Timing diagram: data input/output



Data must always be sampled on the rising edge of the clock

Top page

9.3. High-Speed e•MMC interface timing

Table 9- 2 High speed mode timing

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK(1)					
Clock frequency Data Transfer Mode (PP) (2)	f_{PP}	0	52(3)	MHz	$C_L \leq 30pF$ Tolerance: +100KHz
Clock frequency Identification Mode(OD)	F_{OD}	0	400	KHz	Tolerance: +20KHz
Clock low time / Clock high time	t_{WL}/t_{WH}	6.5	-	ns	$C_L \leq 30pF$
Clock rise time / Clock fall time	t_{TLH}/t_{THL}	-	3	ns	$C_L \leq 30pF$
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3	-	ns	$C_L \leq 30pF$
Input hold time	t_{IH}	3	-	ns	$C_L \leq 30pF$
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data	t_{ODLY}	-	13.7	ns	$C_L \leq 30pF$
Output hold time	t_{OH}	2.5	-	ns	$C_L \leq 30pF$
Signal rise time (5)	t_{rise}	-	3	ns	$C_L \leq 30pF$
Signal fall time	t_{fall}	-	3	ns	$C_L \leq 30pF$

Note* :

1) CLK timing is measured at 50% of VccQ.
2) e•MMC shall support the full frequency range from 0-26MHz, or 0-52MHz.
3) e•MMC can operate as high-speed interface timing at 26MHz clock frequency.
4) CLK rise and fall times are measured by min(VIH) and max(VIL).
5) Inputs CMD,DAT rise and fall times area measured by min(VIH) and max(VIL), and outputs CMD, DAT rise and fall times are measured by min(VOH) and max(VOL).

Top page

9.4. Backward compatible e•MMC interface timing

Table 9- 3 backward-compatible device mode timing

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK(2)					
Clock frequency Data Transfer Mode (PP) (3)	f_{PP}	0	26	MHz	$C_L \leq 30pF$
Clock frequency Identification Mode(OD)	f_{OD}	0	400	KHz	

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock low time / Clock high time	t_{WL}/t_{WH}	10	-	ns	$C_L \leq 30pF$
Clock rise time / Clock fall time	t_{TLH}/t_{THL}	-	10	ns	$C_L \leq 30pF$
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3	-	ns	$C_L \leq 30pF$
Input hold time	t_{IH}	3	-	ns	$C_L \leq 30pF$
Outputs CMD, DAT (referenced to CLK)					
Output set-up time	t_{OSU}	-	13.7	ns	$C_L \leq 30pF$
Output hold time	t_{OH}	2.5	-	ns	$C_L \leq 30pF$

Note* :

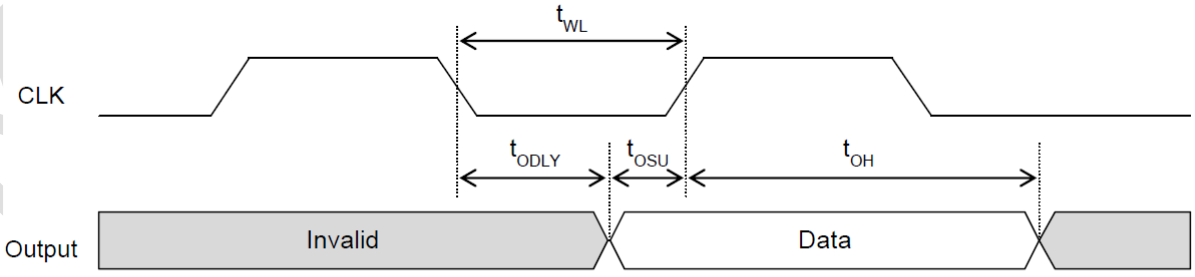
1) The e•MMC must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.
2) CLK timing is measured at 50% of VccQ
3) For compatibility with e•MMCs that support the v4.2 standard or earlier, host should not use >26MHz before switching to high-speed interface timing.
4) tosu and t_{OH} are defined as values from clock rising edge. However, the e•MMC device will utilize clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to set t_{WL} value as long as possible within the range which will not go over t_{CK}-t_{OH}(min) in the system or to use slow clock frequency, so that host could have data set up margin for the device.

use slow clock frequency, so that host could have data set up margin for the device.

MKEV032GCB-SS510 e•MMC device utilize clock falling edge to output data in backward compatibility mode.

Host should optimize the timing in order to have data set up margin as follows.

Figure 9- 2 Output timing



$t_{OSU}(min) = t_{WL}(min) - t_{ODLY}(max\ 8ns)$

Top page

9.5. Bus Timing for DAT Signals During 2X Data Rate Operation

These timings applies to the DAT [7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operates synchronously of both the rising and the falling edges of CLK. the CMD signal still operates synchronously of the rising edge of CLK and therefore complies with the bus timing specified in High-speed interface timing or Backward-compatible interface timing.

Figure 9- 3 Timing diagram: data input/output in dual data rate mode

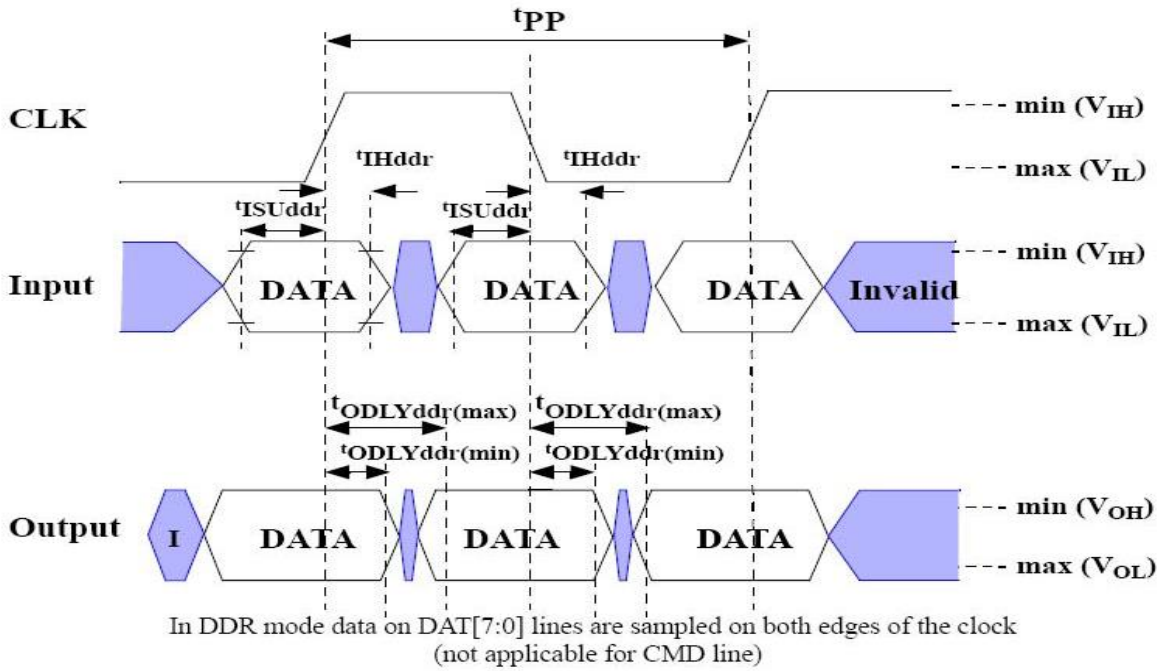


Table9- 4 High-speed dual data rate interface timings

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK(1)					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Inputs DAT (referenced to CLK-DDR mode)					
Input set-up time	t_{ISUDDR}	2.5	-	ns	$C_L \leq 20$ pF
Input hold time	t_{IHDDR}	2.5	-	ns	$C_L \leq 20$ pF
Outputs DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	$t_{ODLYDDR}$	1.5	7	ns	$C_L \leq 20$ pF
Signal rise time(all signal)(2)	t_{RISE}	-	2	ns	$C_L \leq 20$ pF
Signal fall time (all signal)	t_{FALL}	-	2	ns	$C_L \leq 20$ pF

Note* :

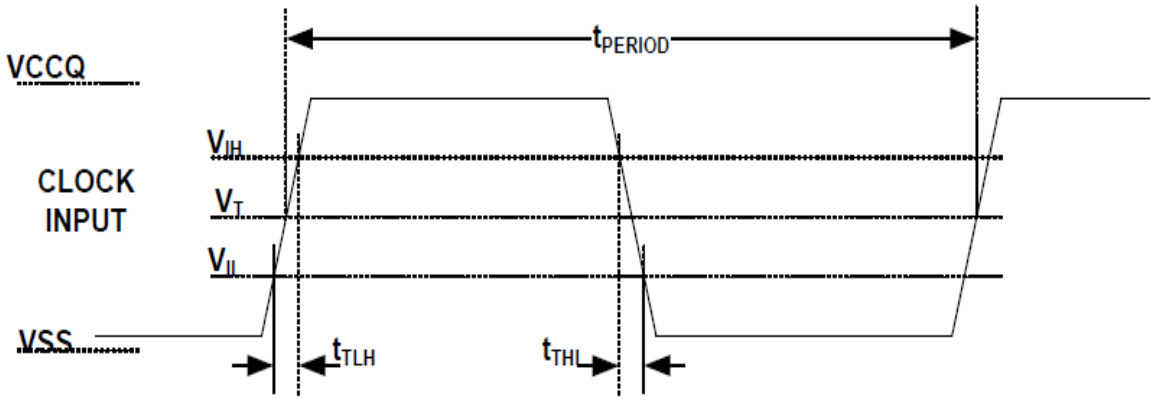
1) CLK timing is measured at 50% of VccQ.
2) Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs CMD, DAT rise and fall times are measured by min (VOH) and max (VOL).

Top page

9.6. Bus Timing Specification in HS200 mode

HS200 Clock Timing

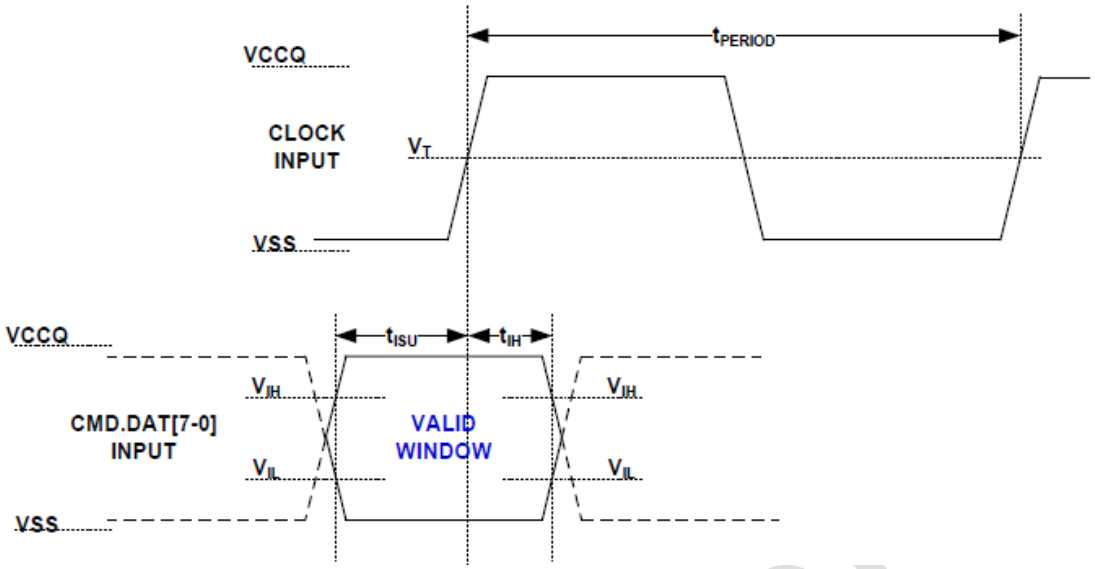
Host CLK Timing in HS200 mode shall conform to the timing specified in following figure and Table. CLK input shall satisfy the clock timing over all possible operation and environment conditions. CLK input parameters should be measured while CMD and DAT lines are stable high or low, as close as possible to the Device. The maximum frequency of HS200 is 200MHz. Hosts can use any frequency up to the maximum that HS200 mode allows.



NOTE 1 VIH denote VIH(min.) and VIL denotes VIL(max.).
NOTE 2 VT=0.975V - Clock Threshold, indicates clock reference point for timing measurements.

Symbol	Min.	Max.	Unit	Remark
tPERIOD	5		ns	200MHz (Max.), between rising edges
tTLH, tTHL		0.2 * tPERIOD	ns	tTLH, tTHL < 1ns (max.) at 200MHz, CDEVICE=6pF,The absolute maximum value of tTLH, tTHL is 10ns regardless of clock frequency.
Duty Cycle	30	70	%	

HS200 Device Input Timing

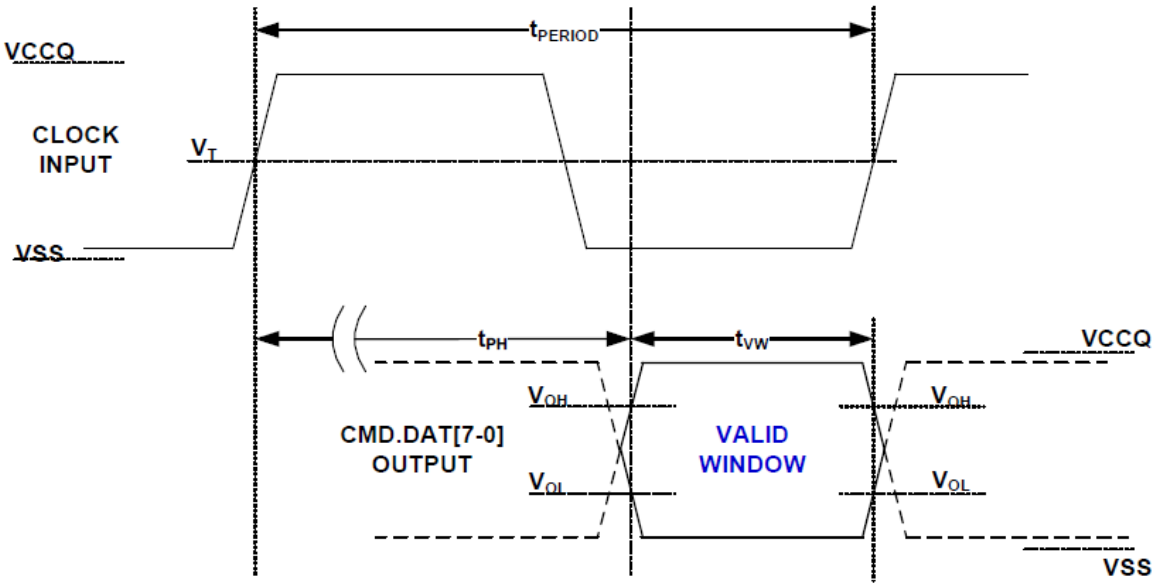


NOTE1 tISU and tIH are measured at VIL(max.)and VIH(min.)
NOTE2 VIH denote VIH(min.) and VIL denotes VIL(max.).

Symbol	Min.	Max.	Unit	Remark
^{t}ISU	1.40		ns	C_{DEVICE} ≤ 6pF
^{t}IH	0.8		ns	C_{DEVICE} ≤ 6pF

HS200 Device Output Timing

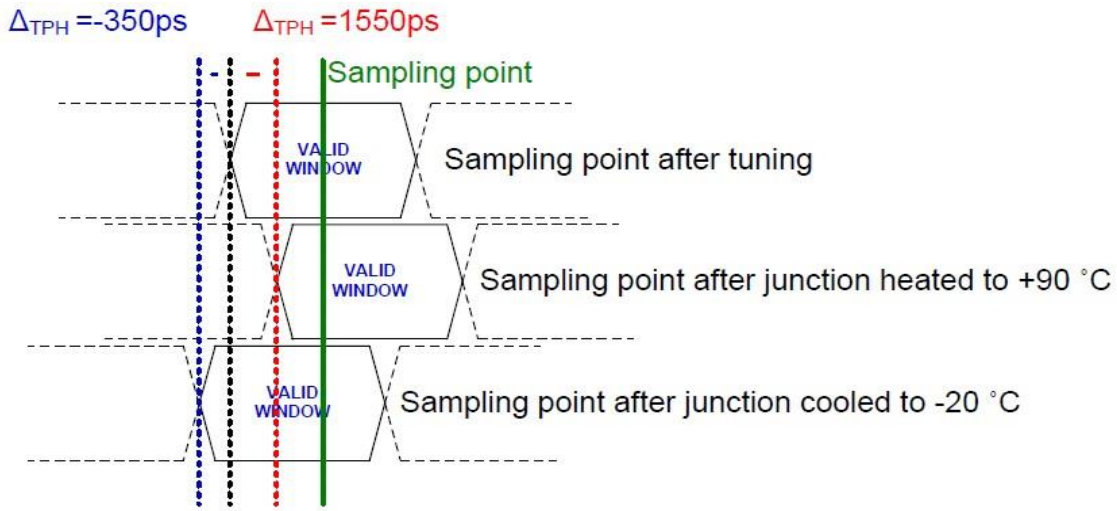
tPH parameter is defined to allow device output delay to be longer than tPERIOD. After initialization, the tPH may have random phase relation to the clock. The Host is responsible to find the optimal sampling point for the Device outputs, while switching to the HS200 mode. While setting the sampling point of data, a long term drift, which mainly depends on temperature drift, should be considered. The temperature drift is expressed by ΔTPH. Output valid data window (tVW) is available regardless of the drift (ΔTPH) but position of data window varies by the drift.



NOTE VOH denotes VOH(min.) and VOL denotes VOL(max.).

Symbol	Min.	Max.	Unit	Remark
tPH	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
ΔTPH	-350 (ΔT = -20 °C)	+1550 (ΔT = 90 °C)	ps	Delay variation due to temperature change after tuning. Total allowable shift of output valid window (TVW) from last system Tuning procedure ΔTPH is 2600ps for ΔT from -25 °C to 125 °C during operation.
tVW	0.575		UI	tVW =2.88ns at 200MHz Using test circuit in following figure including skew among CMD and DAT lines created by the Device. Host path may add Signal Integrity induced noise,skews, etc. Expected tVW at Host input is larger than 0.475UI.

Δ_{TPH} consideration



Implementation Guide:

Host should design to avoid sampling errors that may be caused by the ΔTPH drift.

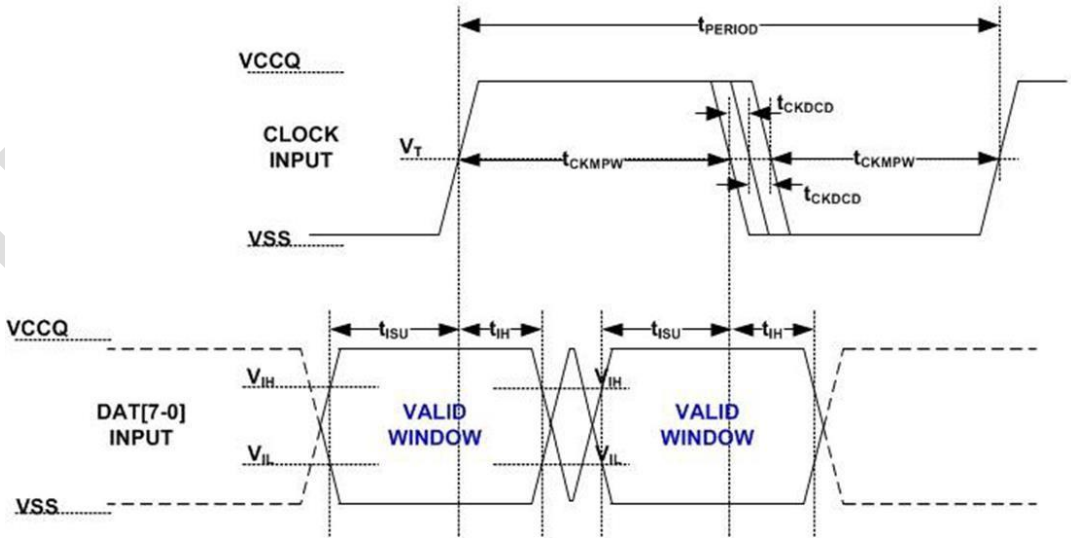
It is recommended to perform tuning procedure while Device wakes up, after sleep. One simple way to overcome the ΔTPH drift is by reduction of operating frequency.

Top page

9.7. Bus Timing Specification in HS400 mode

HS400 Input Timing

The CMD input timing for HS400 mode is the same as CMD input timing for HS200 mode.

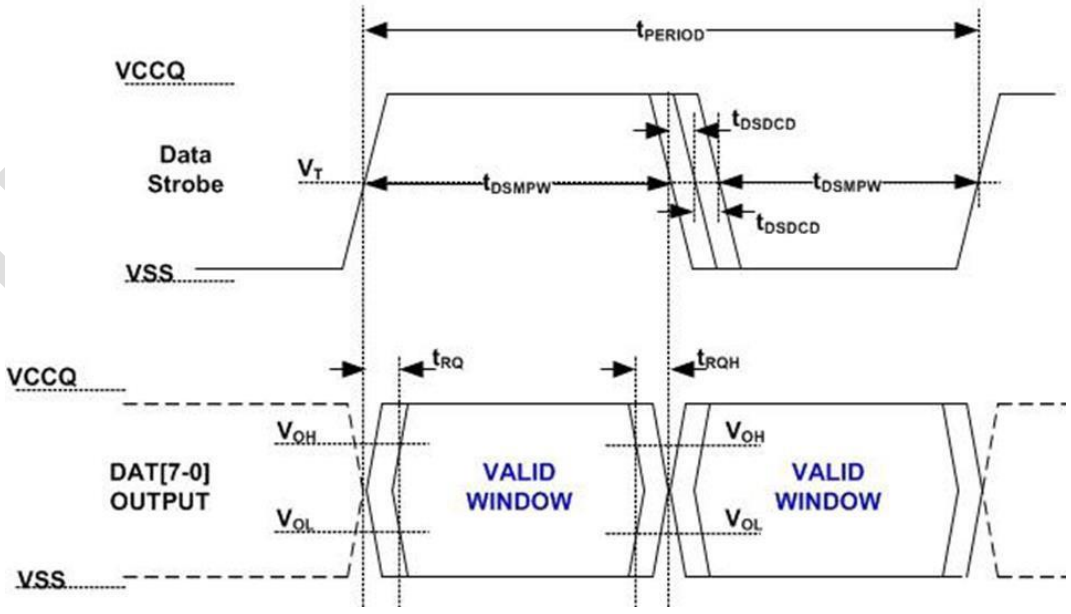


Note : VIH denote VIH(min) and VIL denotes VIL(max)

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CLK					
Cycle time data transfer mode	tPERIOD	5	-	ns	200MHz(Max), between rising edges With respect to VT
Slew rate	SR	1.125	-	V/ns	With respect to V_{IH} /V_{IL}
Duty cycle distortion	tCKDCD	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to VT Includes jitter, phase noise
Minimum pulse width	tCKMPW	2.2	-	ns	With respect to VT
Input DAT(referenced to CLK)					
Input set-up time	tISUddr	0.4	-	ns	CDevice<=6pF With respect to VIH /VIL
Input hold time	tIHddr	0.4	-	ns	CDevice<=6pF With respect to VIH /VIL
Slew rate	SR	1.125	-	V/ns	With respect to VIH /VIL

HS400 Device Output Timing

The Data Strobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC status response.

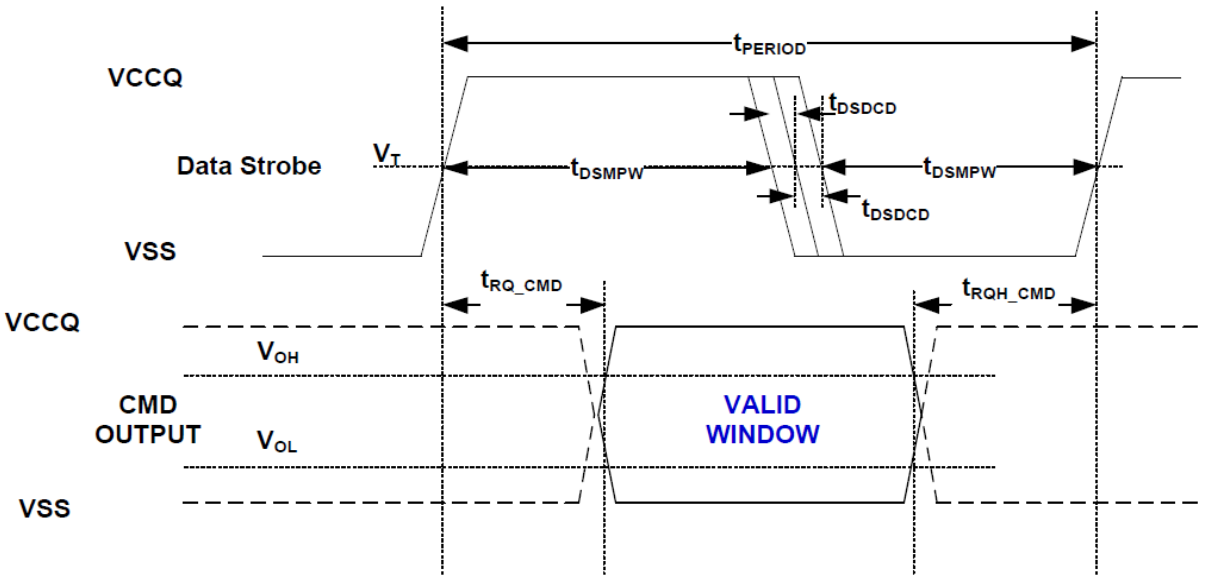


Note : VOH denotes VOH(min) and VOL denotes VOL(max)

Parameter	Symbol	Min.	Max.	Unit	Remark
Data Strobe					
Cycle time data transfer mode	tPERIOD	5	-	ns	200MHz(Max), between rising edges With respect to VT
Slew rate	SR	1.125	-	V/ns	With respect to VOH/VOL and HS400
Duty cycle distortion	tDSDCD	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion(tCKDCD) With respect to VT Includes jitter, phase noise
Minimum pulse width	tDSMPW	2.0	-	ns	With respect to VT
Output DAT(referenced to Data Strobe)					
Output skew	tRQ	-	0.4	ns	With respect to VOH /VOL and HS400
Output hold skew	tRQH	-	0.4	ns	With respect to VOH /VOL and HS400
Slew rate	SR	1.125	-	V/ns	With respect to VOH /VOL and HS400

HS400 Device Command Output Timing

The Data Strobe is used to response of any command in HS400 mode.



Note : VOH denotes VOH(min) and VOL denotes VOL(max)

Parameter	Symbol	Min.	Max.	Unit	Remark
Data Strobe					
Cycle time data transfer mode	tPERIOD	5	-	ns	200MHz(Max), between rising edges With respect to VT
Slew rate	SR	1.125	-	V/ns	With respect to VOH/VOL and HS400 reference load
Duty cycle distortion	tDSDCD	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion(tCKDCD) With respect to VT Includes jitter, phase noise
Minimum pulse width	tDSMPW	2.0	-	ns	With respect to VT
CMD Response (referenced to Data Strobe)					
Output skew(CMD)	tRQ_CMD	-	0.4	ns	With respect to VOH /VOL and HS400 reference
Output hold skew(CMD)	tRQH_CMD	-	0.4	ns	With respect to VOH /VOL and HS400 reference
Slew rate	SR	1.125	-	V/ns	With respect to VOH /VOL and HS400 reference

HS400 Capacitance

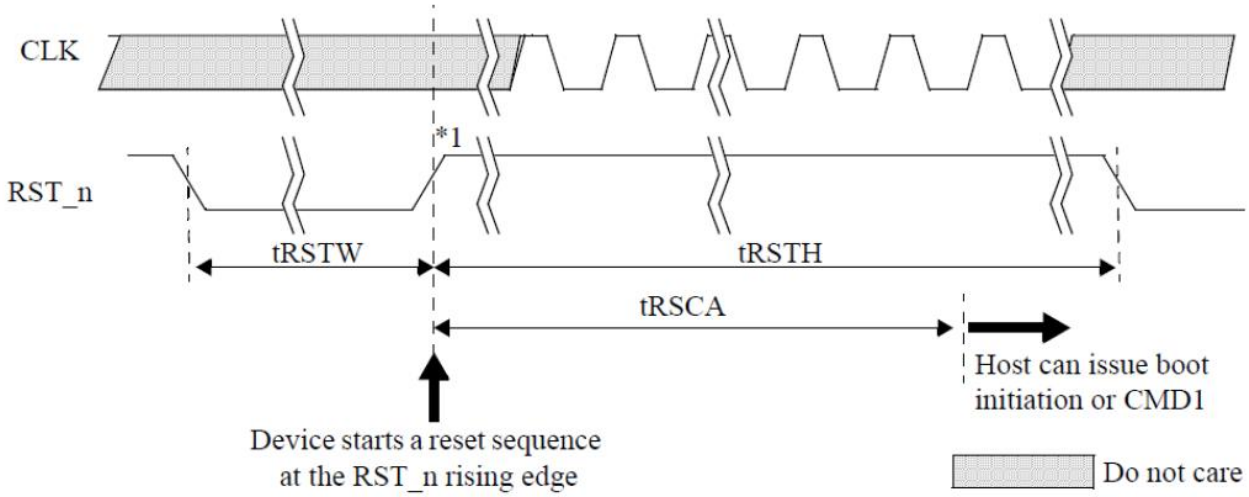
The Data Strobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC s

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7	-	100	KΩ	
Pull-up resistance for DAT0-7	R_{DAT}	10	-	100	KΩ	
Pull-down resistance for Data	R_{DS}	10	-	100	KΩ	
Internal pull up resistance DAT1-DAT7	R_{int}	10	-	150	KΩ	
Bus signal line capacitance	C_L	-	-	13	pF	
Single Device capacitance	C_{DEVICE}	-	-	6	pF	

Top page

9.8. H/W Reset operation

Device will detect the rising edge of RST_n signal to trigger internal reset sequence.



Note1: Device will detect the rising edge of RST_n signal to trigger internal reset sequence

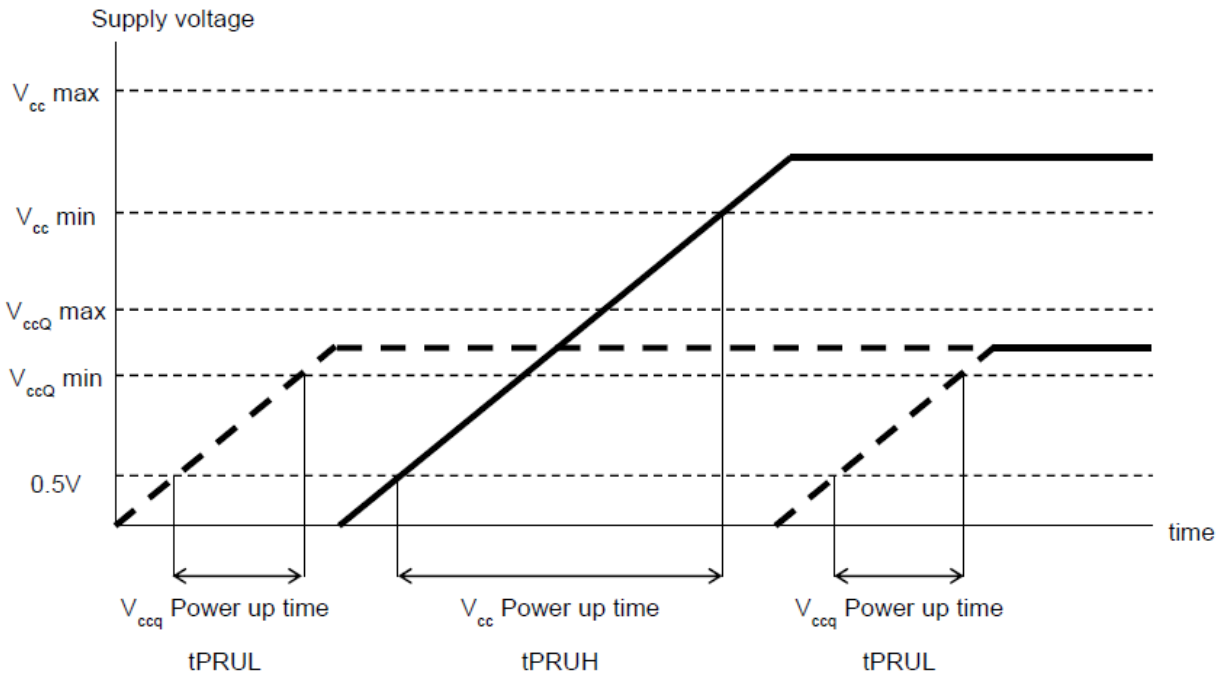
H/W Reset Timings

Parameter	Symbol	Test Conditions	Min.	Max.	Unit
RST_n pulse width	tRSTW		1		μs
RST_n to Command time	tRSCA		200[1]		μs
RST_n high period (interval time)	tRSTH		1		μs

1) 74 cycles of clock signal required before issuing CMD1 or CMD0 with argument 0xFFFFFFFA
2) During the device internal initialization sequence right after power on, device may not be able to detect RST_n signal, because the device may not complete loading RST_n_ENABLE bits of the extended CSD register into the controller yet.

Top page

9.9. Power-up sequence



Power-up parameter

Parameter	Symbol	Test Conditions	Min.	Max.	Remark
Supply power-up for 3.3V	tPRUH		5 μs	35 ms	
Supply power-up for 1.8V	tPRUL		5 μs	25 ms	

Top page

10. Device Register

10.1. CID Register

The Card Identification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual flash or I/O card shall have a unique identification number. Every type of ROM cards (defined by content) shall have a unique identification number. The structure of the CID register is defined in the following sections.

Table 10- 1 CID Table

Name	Field	Width	CID-slice	CID Value
Manufacture ID	MID	8	[127:120]	EAh
Reserved	-	6	[119:114]	0h
Card/BGA	CBX	2	[113:112]	01h
OEM/Application ID	OID	8	[111:104]	0Eh
Product name	PNM	48	[103:56]	53 50 65 4D 4D 43(SPeMMC)
Product revision	PRV	8	[55:48]	10h
Product serial number	PSN	32	[47:16]	Serial number
Manufacturing date	MDT	8	[15:8]	Manufacturing date
CRC7 checksum	CRC	7	[7:1]	CRC
Not used, always '1'	-	1	[0:0]	1h

Top page

10.2. OCR Register

The 32-bit operation conditions register stores the VCCQ voltage profile of the e•MMC In addition, this register includes a status information bit. This status bit is set if the e•MMC power up procedure has been finished. The OCR register shall be implemented by e•MMC.

Table 10- 2 OCR Table

OCR bit	VCCQ voltage window	eMMC
[31]	power up status bit (busy)*	
[30:29]	Access Mode	00b (byte mode) 10b (sector mode)
[28:24]	Reserved	0 0000b
[23:15]	2.7V – 3.6V	1 1111 1111 b
[14:8]	2.0V – 2.6V	000 0000b
[7]	1.7V~1.95V	1b
[6:0]	Reserved	000 0000b

Note* :
This bit is set to LOW if the e•MMC has not finished the power up routine.
The supported voltage range is coded as shown in table.

Top page

10.3. CSD Register

The Card-Specific Data (CSD) register provides information on how to access the card contents. The CSD defines the data format, error correction type, maximum data access time; data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the CSD Registry entries coded as follows:

Table 10- 3 CSD Table

Name	Field	Width	Cell Type	CSD-slice	CSD Value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	3h
System specification version	SPEC_VERS	4	R	[125:122]	4h
Reserved	-	2	R	[121:120]	0h
Data read access-time 1	TAAC	8	R	[119:112]	7Fh
Data read access-time 2	NSAC	8	R	[111:104]	8h
Max. data transfer rate	TRAN_SPEED	8	R	[103:96]	32h
Device command classes	CCC	12	R	[95:84]	5F5h
Max. read data block length	READ_BL_LEN	4	R	[83:80]	9h
Partial block read allowed	READ_BL_PARTIAL	1	R	[79]	0h
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78]	0h
Read block misalignment	READ_BLK_MISALIGN	1	R	[77]	0h
DSR implemented	DSR_IMP	1	R	[76]	0h

Name	Field	Width	Cell Type	CSD-slice	CSD Value
Reserved	-	2	R	[75:74]	0h
Device size	C_SIZE	12	R	[73:62]	FFFh
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	6h
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	6h
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	6h
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	6h
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	7h
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	1Fh
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1Fh
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	Fh
Write protect group enable	WP_GRP_ENABLE	1	R	[31]	1h
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0h
Write speed factor	R2W_FACTOR	3	R	[28:26]	5h
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	9h
Partial block write allowed	WRITE_BL_PARTIAL	1	R	[21]	0h
Reserved	-	4	R	[20:17]	0h
Content protection application	CONTENT_PROT_APP	1	R	[16]	0h
File format group	FILE_FORMAT_GRP	1	R/W	[15]	0h
Copy flag (OTP)	COPY	1	R/W	[14]	0h
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13]	0h
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12]	0h
File format	FILE_FORMAT	2	R/W	[11:10]	0h
ECC code	ECC	2	R/W/E	[9:8]	0h
CRC	CRC	7	R/W/E	[7:1]	0h
Not used, always '1'	-	1	-	[0]	1h

Top page

10.4. Extended CSD Register

The Extended CSD register defines the card properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the card capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the card is working in. These modes can be changed by the host by means of the SWITCH command.

Multi bytes field is interpreted in little endian byte order.

R: Read only.

W: One time programmable and not readable.

R/W: One time programmable and readable.

W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.

R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.

R/W/C_P: Writable after value cleared by power failure and HW/rest assertion (the value not cleared by CMD0 reset) and readable.

R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.

W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

Table 10- 4 Extended CSD Table

Name	Field	Size	Cell Type	CSD Slice	Value
Reserved	-	6	TBD	[511:506]	0h
Extend Security Command Error	EXT_SECURITAY	1	R	[505]	0h
Supported Command Sets	S_CMD_SET	1	R	[504]	1h
HPI features	HPI_FEATURES	1	R	[503]	1h
Background operations support	BKOPS_SUPPORT	1	R	[502]	1h
Max packed read commands	MAX_PACKED_READS	1	R	[501]	Ah
Max packed write commands	MAX_PACKED_WRITES	1	R	[500]	Ah
Data Tag Support	DATA_TAG_SUPPORT	1	R	[499]	1h
Tag Unit Size	TAG_UNIT_SIZE	1	R	[498]	5h
Tag Resources Size	TAG_RES_SIZE	1	R	[497]	1h
Context management capabilities	CONTEXT_CAPABILITIES	1	R	[496]	5h
Large Unit size	LARGE_UNIT_SIZE_M1	1	R	[495]	7h
Extended partitions attribute support	EXT_SUPPORT	1	R	[494]	3h
Supported modes	SUPPORTED_MODES	1	R	[493]	3h
FFU features	FFU_FEATURES	1	R	[492]	1h
Operation codes timeout	OPERATION_CODE_TIMEOUT	1	R	[491]	40h

Name	Field	Size	Cell Type	CSD Slice	Value
FFU Argument	FFU_ARG	4	R	[490:487]	0h
Barrier support	BARRIER_SUPPORT	1	R	[486]	0h
Reserved	-	177	TBD	[485:309]	ALL"0"
CMD Queuing Support	CMDQ_SUPPORT	1	R	[308]	1h
CMD Queuing Depth	CMDQ_DEPTH	1	R	[307]	1Fh
Reserved	-	1	TBD	[306]	0h
Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	R	[305:302]	0h
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	[301:270]	All "0"
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	[269]	0h
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	[268]	0h
Pre EOL information	PRE_EOL_INFO	1	R	[267]	0h
Optimal read size	OPTIMAL_READ_SIZE	1	R	[266]	1h
Optimal write size	OPTIMAL_WRITE_SIZE	1	R	[265]	1h
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	[264]	1h
Device version	DEVICE_VERSION	2	R	[263:262]	0h
Firmware version	FIRMWARE_VERSION	8	R	[261:254]	0h
Power class for 200MHz, DDR at VCC= 3.6V	PWR_CL_DDR_200_360	1	R	[253]	0h
Cache size	CACHE_SIZE	4	R	[252:249]	0h
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	[248]	40h
Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	2h
Background operations status	BKOPS_STATUS	1	R	[246]	0h
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0h
Number of correctly programmed sectors	INI_TIMEOUT_AP	1	R	[241]	Ah
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	R	[240]	0h
Power class for 52MHz, DDR at VCC = 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0h

Name	Field	Size	Cell Type	CSD Slice	Value
Power class for 52MHz, DDR at VCC = 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0h
Power class for 200MHz at VCCQ =1.95V, VCC = 3.6V	PWR_CL_200_195	1	R	[237]	0h
Power class for 200MHz, at VCCQ =1.3V, VCC = 3.6V	PWR_CL_200_130	1	R	[236]	0h
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0h
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0h
Reserved	-	2	TBD	[233]	0h
TRIM Multiplier	TRIM_MULT	1	R	[232]	10h
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	[231]	55h
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	1Bh
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	11h
Boot information	BOOT_INFO	1	R	[228]	7h
Reserved	-	1	TBD	[227]	0h
Boot partition size	BOOT_SIZE_MULT	1	R	[226]	20h
Access size	ACC_SIZE	1	R	[225]	6h
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	1h
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	10h
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	1h
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	10h
Sleep current (VCC)	S_C_VCC	1	R	[220]	Dh
Sleep current (VCCQ)	S_C_VCCQ	1	R	[219]	Dh
Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMOUT	1	R	[218]	6h
Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	17h
Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME	1	R	[216]	0h
Sector Count	SEC_COUNT	4	R	[215:212]	39EF6C0h
Secure Write Protect Information	SECURE_WP_INFO	1	R	[211]	0h

Name	Field	Size	Cell Type	CSD Slice	Value
Minimum Write Performance for 8bit at 52 MHz	MIN_PERF_W_8_52	1	R	[210]	0h
Minimum Read Performance for 8bit at 52 MHz	MIN_PERF_R_8_52	1	R	[209]	0h
Minimum Write Performance for 8bit at 26 MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0h
Minimum Read Performance for 8bit at 26 MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0h
Minimum Write Performance for 4bit at 26 MHz	MIN_PERF_W_4_26	1	R	[206]	0h
Minimum Read Performance for 4bit at 26 MHz	MIN_PERF_R_4_26	1	R	[205]	0h
Reserved	-	1	TBD	[204]	0h
Power class for 26 MHz at 3.6 V 1 R	PWR_CL_26_360	1	R	[203]	0h
Power class for 52 MHz at 3.6 V 1 R	PWR_CL_52_360	1	R	[202]	0h
Power class for 26 MHz at 1.95 V 1 R	PWR_CL_26_195	1	R	[201]	0h
Power class for 52 MHz at 1.95 V 1 R	PWR_CL_52_195	1	R	[200]	0h
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	FFh
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	64h
I/O Driver Strength	DRIVER_STRENGTH	1	R	[197]	0h
Device type	DEVICE_TYPE	1	R	[196]	57h
Reserved	-	1	TBD	[195]	0h
CSD STRUCTURE	CSD_STRUCTURE	1	R	[194]	2h
Reserved	-	1	TBD	[193]	0h
Extended CSD revision	EXT_CSD_REV	1	R	[192]	8h
Modes Segment					
Command set	CMD_SET	1	R/W/E_P	[191]	0h
Reserved	-	1	TBD	[190]	0h
Command set revision	CMD_SET_REV	-	R	[189]	0h
Reserved	-	1	TBD	[188]	0h

Name	Field	Size	Cell Type	CSD Slice	Value
Power class	POWER_CLASS	-	R/W/E_P	[187]	0h
Reserved	-	1	TBD	[186]	0h
High-speed interface timing	HS_TIMING	1	R/W/E_P	[185]	2h
Strobe Support	STROBE_SUPPORT	1	TBD	[184]	0h
Bus width mode	BUS_WIDTH	1	W/E_P	[183]	2h
Reserved	-	1	TBD	[182]	0h
Erased memory content	ERASED_MEM_CONT	1		[181]	0h
Reserved	-	1	TBD	[180]	0h
Partition configuration	PARTITION_CONFIG	1	R/W/E & E/W/E_P	[179]	0h
Boot config protection	BOOT_CONFIG_PROT	1	R/W & R/W/C_P	[178]	0h
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	[177]	0h
Reserved	-	1	TBD	[176]	0h
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E	[175]	0h
Boot write protection status registers	BOOT_WP_STATUS	1	R	[174]	0h
Boot area write protection register	BOOT_WP	1	R/W & R/W/C_P	[173]	0h
Reserved	-	1	TBD	[172]	0h
User area write protection register	USER_WP	1	R/W, R/W/C_P & R/W/E_P	[171]	0h
Reserved	-	1	TBD	[170]	0h
FW configuration	FW_CONFIG	1	R/W	[169]	0h
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	20h
Write reliability setting register	WR_REL_SET	1	R/W	[167]	1Fh
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	14h
Start Sanitize operation	SANITIZE_START	1	W/E_P	[165]	0h
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0h
Enable background operations handshake	BKOPS_EN	1	R/W & R/W/E	[163]	0h
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0h

Name	Field	Size	Cell Type	CSD Slice	Value
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0h
Partitioning Support	PARTITIONING_SUPPORT	1	R	[160]	7h
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	4D3h
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0h
Partitioning Setting	PARTITION_SETTING_COMPLETED	1	R/W	[155]	0h
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	0h
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	0h
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0h
Reserved	-	1	TBD	[135]	0h
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	[134]	0h
Production state awareness	PRODUCTION_STATE_AWARENESS	1	R/W/E	[133]	0h
Package Case Temperature is controlled	TCASE_SUPPORT	1	W/E_P	[132]	0h
Periodic Wake-up	PERIODIC_WAKEUP	1	R/W/E	[131]	0h
Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	[130]	0h
Reserved	-	2	TBD	[129:128]	0h
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	<vendor specific>	[127:64]	0h
Native sector size	NATIVE_SECTOR_SIZE	1	R	[63]	0h
Sector size emulation	USE_NATIVE_SECTOR	1	R/W	[62]	0h
Sector size	DATA_SECTOR_SIZE	1	R	[61]	0h
1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	[60]	0h
Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	[59]	0h
Number of addressed group to be Released	DYNCAP_NEEDED	1	R	[58]	0h
Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	[57:56]	0h
Exception events status	EXCEPTION_EVENTS_STATUS	2	R	[55:54]	0h

Name	Field	Size	Cell Type	CSD Slice	Value
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE	2	R/W	[53:52]	0h
Context configuration	CONTEXT_CONF	15	R/W/E_P	[51:37]	0h
Packed command status	PACKED_COMMAND_STATUS	1	R	[36]	0h
Packed command failure index	PACKED_FAILURE_INDEX	1	R	[35]	0h
Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	0h
Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	[33]	0h
Flushing of the cache	FLUSH_CACHE	1	W/E_P	[32]	0h
Control to turn the Barrier ON/OFF	BARRIER_CTRL	1	R/W	[31]	0h
Mode config	MODE_CONFIG	1	R/W/E_P	[30]	0h
Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	[29]	0h
Reserved	-	2	TBD	[28:27]	0h
FFU status	FFU_STATUS	1	R	[26]	0h
Pre loading data size	PRE_LOADING_DATA_SIZE	4	R/W/E_P	[25:22]	0h
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	R	[21:18]	E7BDB0h
Product state awareness enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E & R	[17]	3h
Secure Removal Type	SECURE_REMOVAL_TYPE	1	R/W & R	[16]	1h
Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	[15]	0h
Reserved	-	15	TBD	[14:0]	0h

Notes:
Reserved bits should be read as 0.

Top page